Mini PCI Express™ Card Electromechanical Specification Revision 1.0

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1. Introduction

1.1. Overview

This specification defines an implementation for small form factor PCI Express cards. Mini PCI Express uses a qualified sub-set of the same signal protocol, electrical definitions, and configuration definitions as the *PCI Express Base Specification, Revision 1.0*. Where this specification does not explicitly define PCI Express characteristics, the *PCI Express Base Specification* governs.

The primary differences between a PCI Express add-in card (as defined by the *PCI Express Card Electromechanical Specification*) and a Mini PCI Express add-in card is a unique card form factor optimized for mobile computing platforms and a card-system interconnection optimized for communication applications. Specifically, Mini PCI Express add-in cards are smaller and have smaller connectors than standard PCI Express add-in cards.

Figure 1-1 shows a conceptual drawing of this form factor as it may be installed in a mobile platform. Figure 1-1 does not reflect the actual dimensions and physical characteristics as those details are specified elsewhere in this specification. However, it is representative of the general concept of this specification to use a single system connector to support all necessary system interfaces by means of a common edge connector. Communications media interfaces may be provided via separate I/O connectors and RF connectors each with independent cables as illustrated in Figure 1-1.

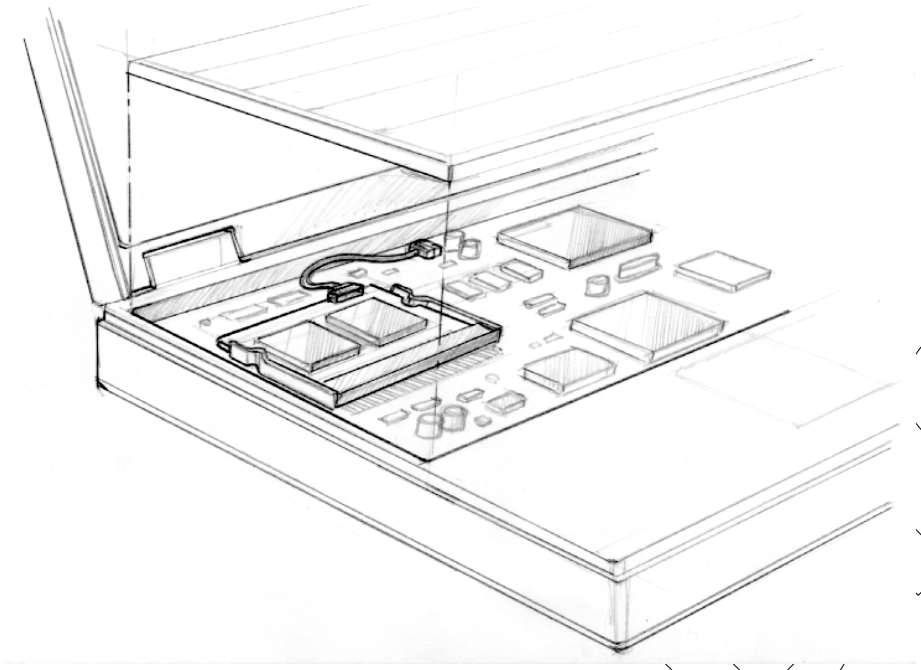

Figure 1-1: Mini PCI Express Add-in Card Installed in a Mobile Platform

Mini PCI Express supports two primary system bus interfaces: PCI Express and USB as shown in Figure 1-2.

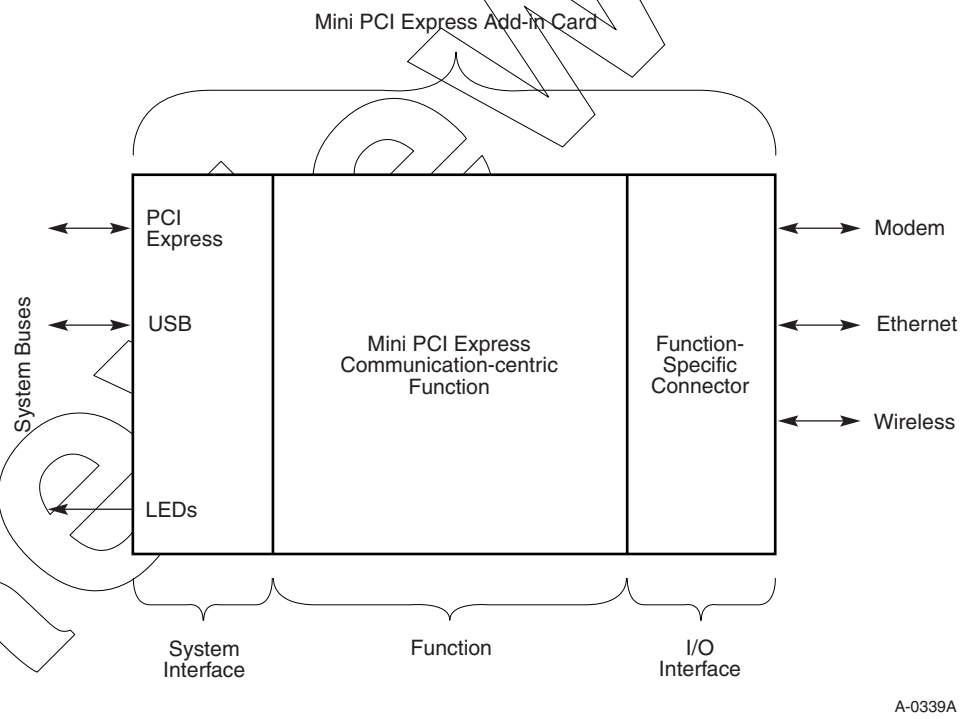

Figure 1-2: Logical Representation of the Mini PCI Express Specification

1.2. Specification References

This specification requires references to other specifications or documents that will form the basis for some of the requirements stated herein.

- *PCI Express Base Specification, Revision 1.0*
- *PCI Express Card Electromechanical Specification, Revision 1.0*
- *PCI Local Bus Specification, Revision 2.3*
- *Mini PCI Specification, Revision 1.0*
- *Universal Serial Bus Specification, Revision 2.0*
- *SMBus Specification, Revision 2.0*
- *EIA-364-1000.01: Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications*
- *EIA-364: Electrical Connector/Socket Test Procedures Including Environmental Classifications*

1.3. Targeted Applications

Although Mini PCI Express is originally intended for both wired and wireless communication applications, it is not limited to such applications. Communications-specific applications may include:

Wired data communication:

- Local Area Network (LAN): 10/100/1000 Mbps Ethernet
- Wide Area Network (WAN): V.90/V.92 modem

Wireless data communication:

- Wireless-LAN (W-LAN): 802.11b/g/a (2.4 GHz and 5.2 GHz bands)
- Wireless-WAN (W-WAN): Cellular data (e.g., GSM/GPRS, UMTS, and CDMA-2000)
- Wireless-Personal Area Network (W-PAN): Bluetooth

Mini PCI Express is targeted toward addressing system manufacturers' needs for build-to-order and configure-to-order rather than providing a general end-user-replaceable module. In specific applications such as wireless, there are worldwide regulatory implications in providing end-user access to items such as antenna connections and frequency-determining components. It is up to the system manufacturer to limit access to appropriate trained service personnel and provide such notification to the user.

Although not specifically considered, other applications that may also find their way to this form factor include advanced wired WAN technologies (xDSL and cable modem), location services using GPS, and audio functions.

1.4. Features and Benefits

The performance characteristics of PCI Express make Mini PCI Express add-in cards desirable in a wide range of mobile systems. This mobile computer optimized form factor provides a number of benefits, including:

- **Upgradeability –** Mini PCI Express add-in cards are removable and upgradeable with available "new technology" cards. This allows upgrades to the newest technologies. System manufacturers are responsible for providing sufficient notification in the accompanying manual when a qualified technician should perform the upgrade service.
- **Flexibility –** A single Mini PCI Express interface can accommodate various types of communications devices. Therefore, the OEM manufacturer can supply build-to-order systems (for example, a network interface card instead of a modem or Token Ring instead of Ethernet).
- **Reduced Cost –** A standard form factor for small form factor add-in cards makes them more manufacturable, which may lead to reduced costs and provide an economy-of-scale advantage over custom manufactured form factors.
- **Serviceability –** Mini PCI Express add-in cards can be removed and easily serviced if they fail.
- **Reliability –** Mini PCI Express add-in cards will be mass-produced cards with higher quality than low-volume custom boards.
- **Software Compatibility –** Mini PCI Express add-in cards are intended to be fully compatible with software drivers and applications that will be developed for standard PCI Express add-in cards.
- **Reduced Size –** Mini PCI Express add-in cards are smaller than PC Cards, PCI Express add-in cards, Mini PCI add-in cards, and other add-in card form factors. This reduced size permits a higher level of integration of data communications devices into notebook PCs.
- **Regulatory Agency Accepted Form Factor –** Standardization of the Mini PCI Express-form factor will permit world wide regulatory agencies to approve Mini PCI Express communications devices independent of the system. This significantly reduces cost and risk on the part of systems manufacturers.
- **Power Management –** Mini PCI Express is designed to be truly mobile friendly for current and future mobile specific power management features.

2

2. Mechanical Specification

2.1. Overview

This specification defines a small form factor card for systems in which a PCI Express add-in card cannot be used due to mechanical system design constraints. The specification defines a smaller card based on a single 52-pin card-edge type connector for system interfaces. The specification also defines the Mini PCI Expresssystem board connector.

2.2. Card Specifications

There is one Mini PCI Express add-in card size.

For purposes of the drawings in this specification, the following notes apply:

- All dimensions are in millimeters, unless otherwise specified.
- All dimension tolerances are ± 0.15 mm, unless otherwise specified.
- Dimensions marked with an asterisk (*) are overall envelope dimensions and include space allowances for insulation to comply with regulatory and safety requirements.
- Insulating material shall not interfere with or obstruct mounting holes or grounding pads.

2.2.1. Card Form Factor

The card form factor is specified by Figure 2-1. The figure illustrates a modem example application. The hatched area shown in this figure represents the available component volume for the card's circuitry.

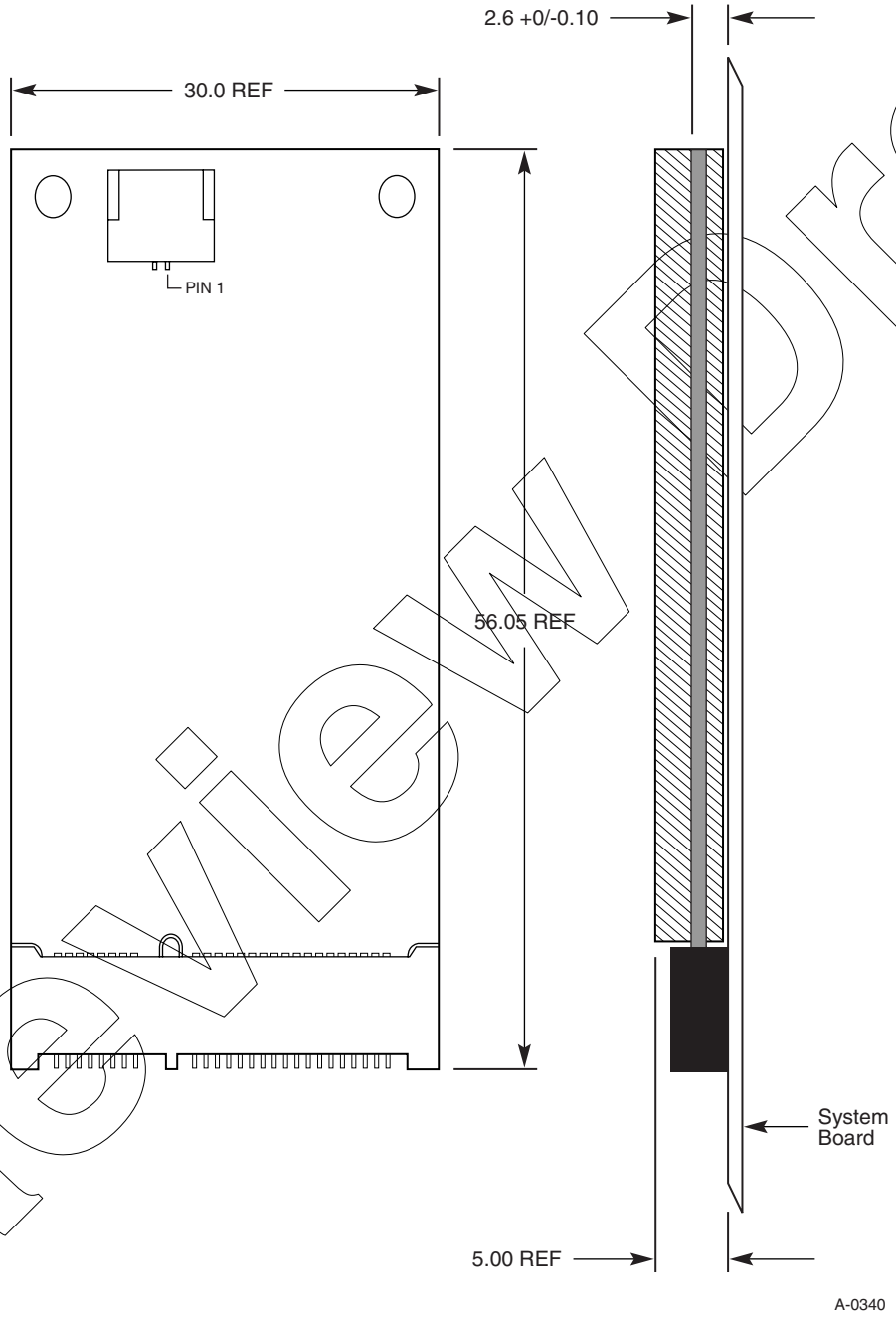

Figure 2-1: Card Form Factor (Modem Example Application Shown)

2.2.2. Card PCB Details

Figure 2-2, Figure 2-3, Figure 2-4, and Figure 2-5 provide the printed circuit board (PCB) details required to fabricate the card. The PCB for this application is expected to be 1.0 mm thick.

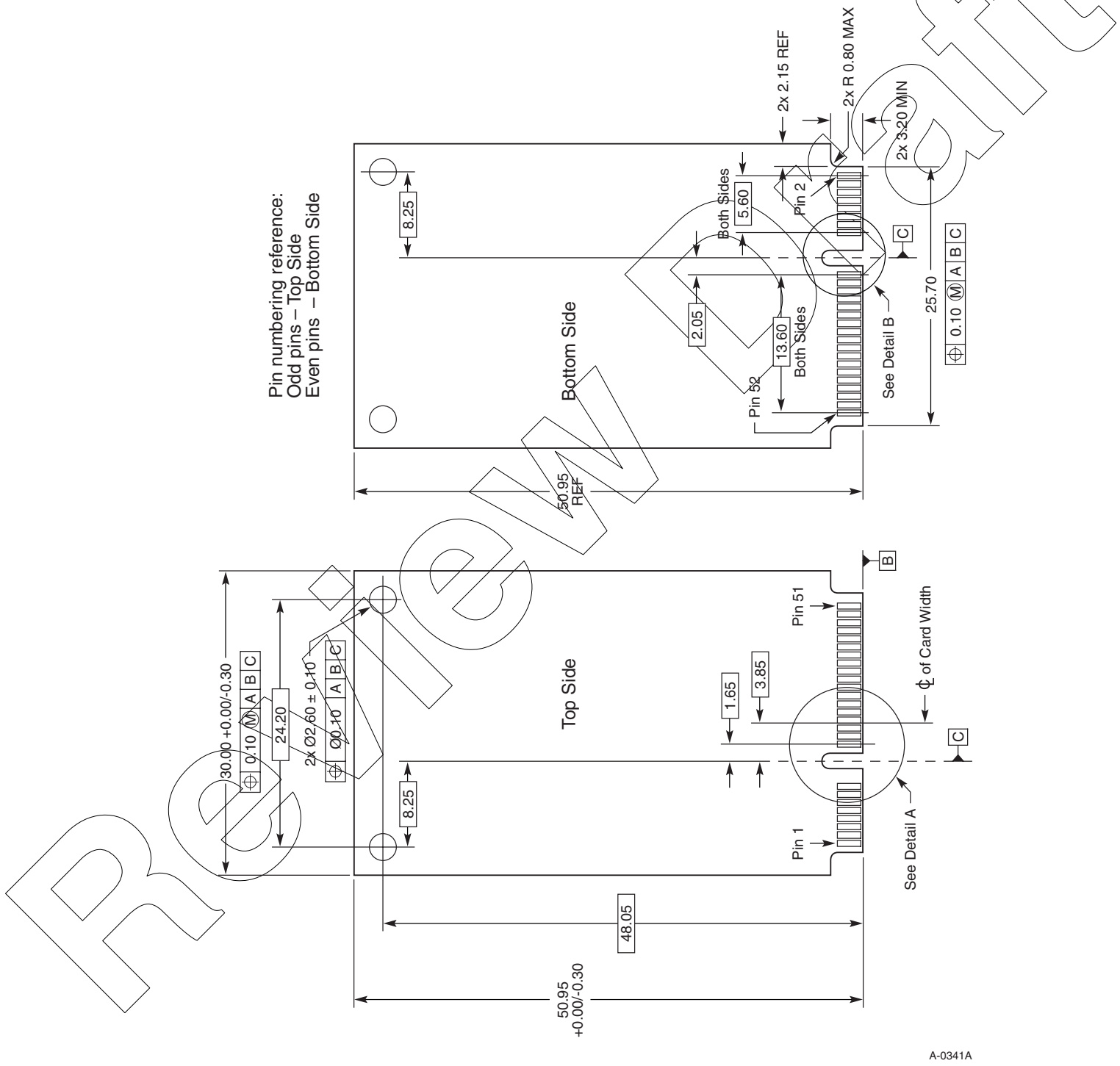

Figure 2-2: Card Top and Bottom

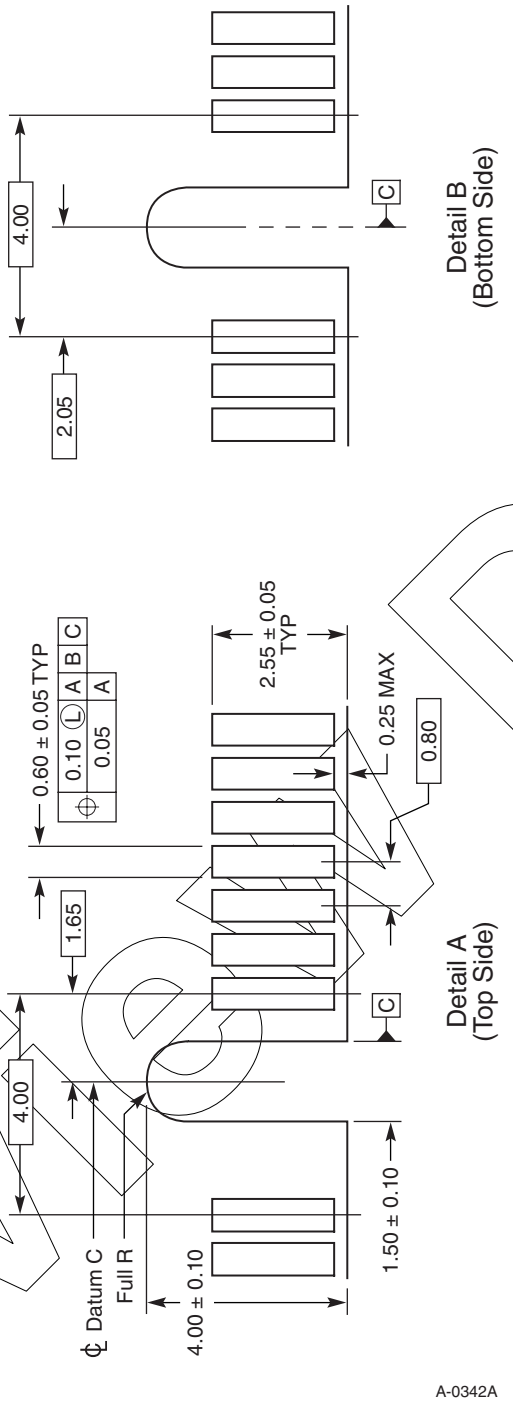

Figure 2-3: Card Top and Bottom Details A and B

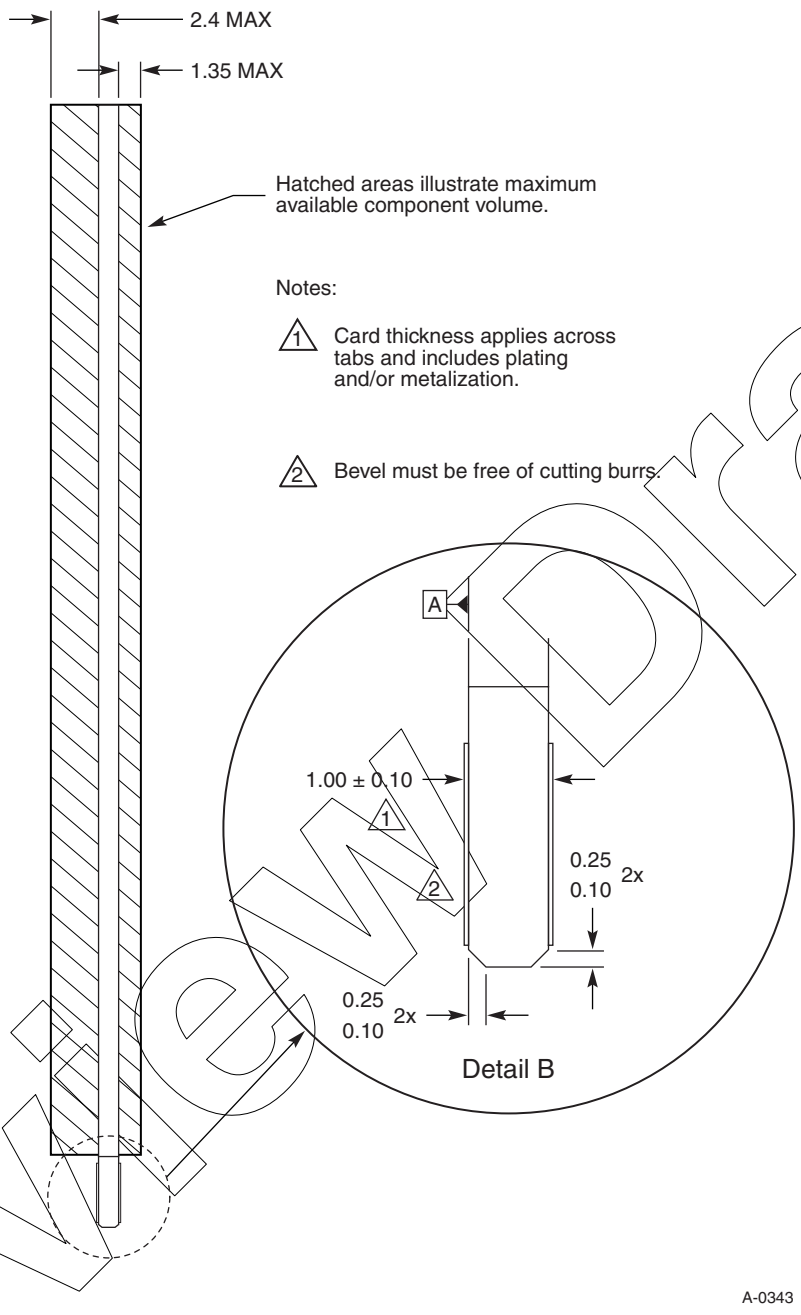

Figure 2-4: Card Edge

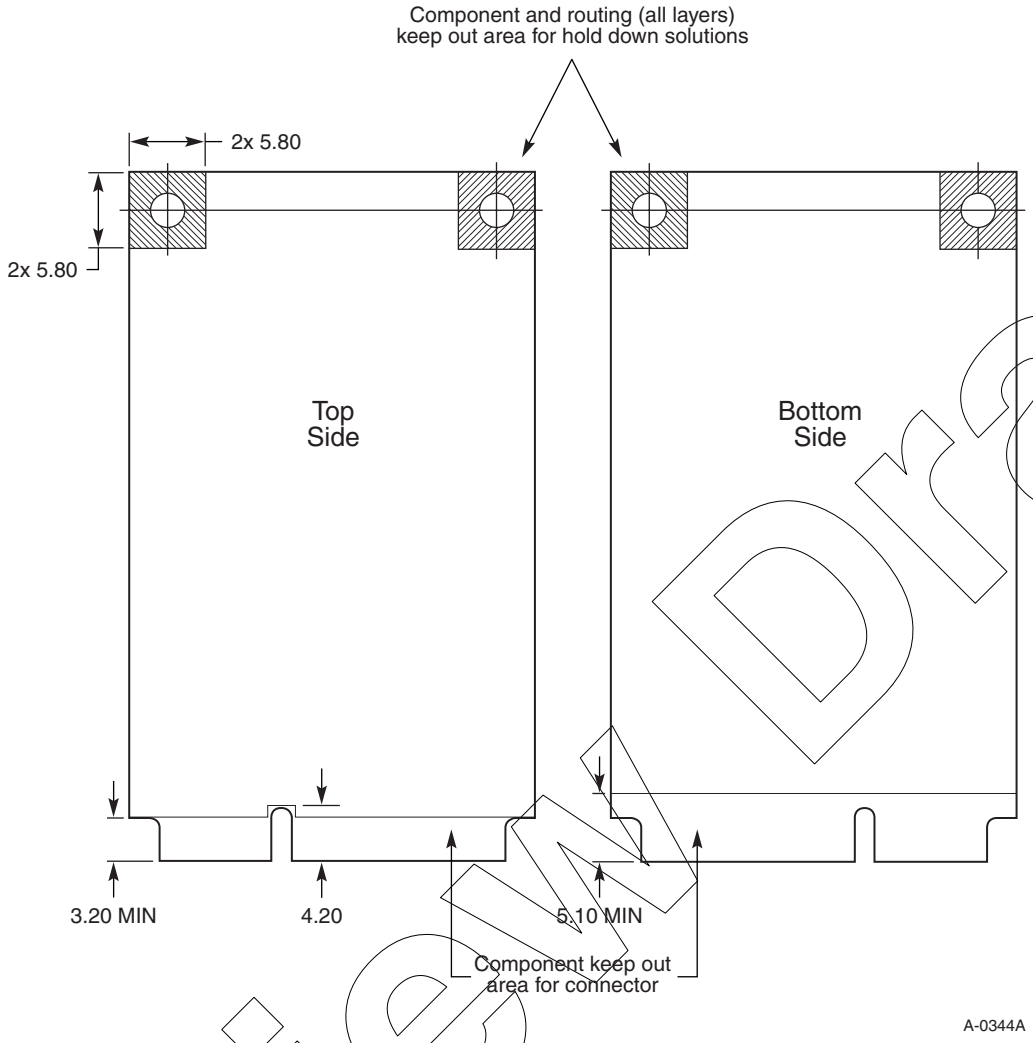

Figure 2-5: Card Component Keep Out Areas

2.3. System Connector Specifications

The Mini PCI Express system connector is similar to the SO-DIMM connector and is modeled after the Mini PCI Type III connector without side retaining clips.

Note: All dimensions are in millimeters, unless otherwise specified. All dimension tolerances are ± 0.15 mm, unless otherwise specified.

2.3.1. System Connector

The system connector is 52-pin card edge type connector. Detailed dimensions should be obtained from the connector manufacturer. Figure 2-6 shows the system connector. Figure 2-7, Figure 2-8, and Figure 2-9 show the recommended locations of the Mini PCI Express system connector on the system board.

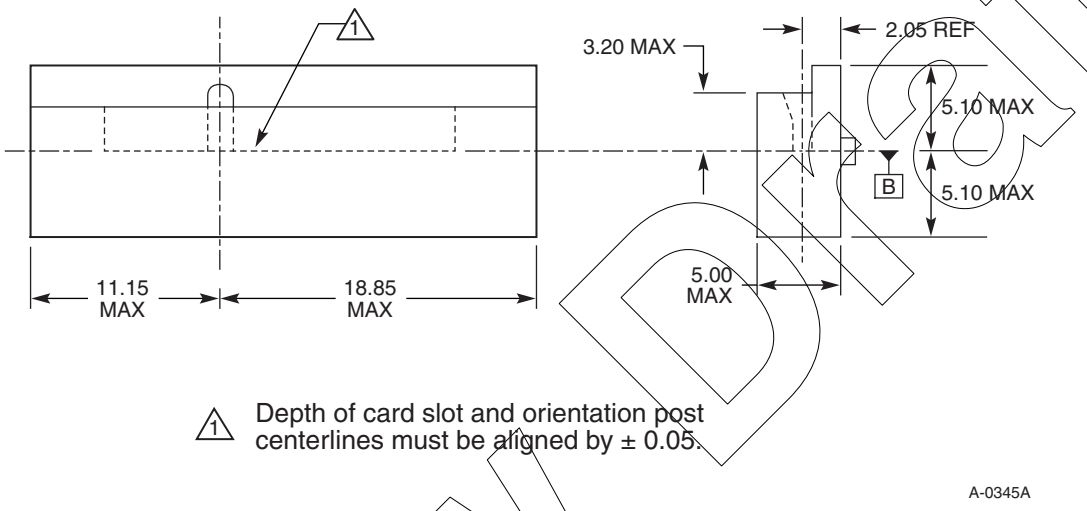

Figure 2-6: Mini PCI Express System Connector

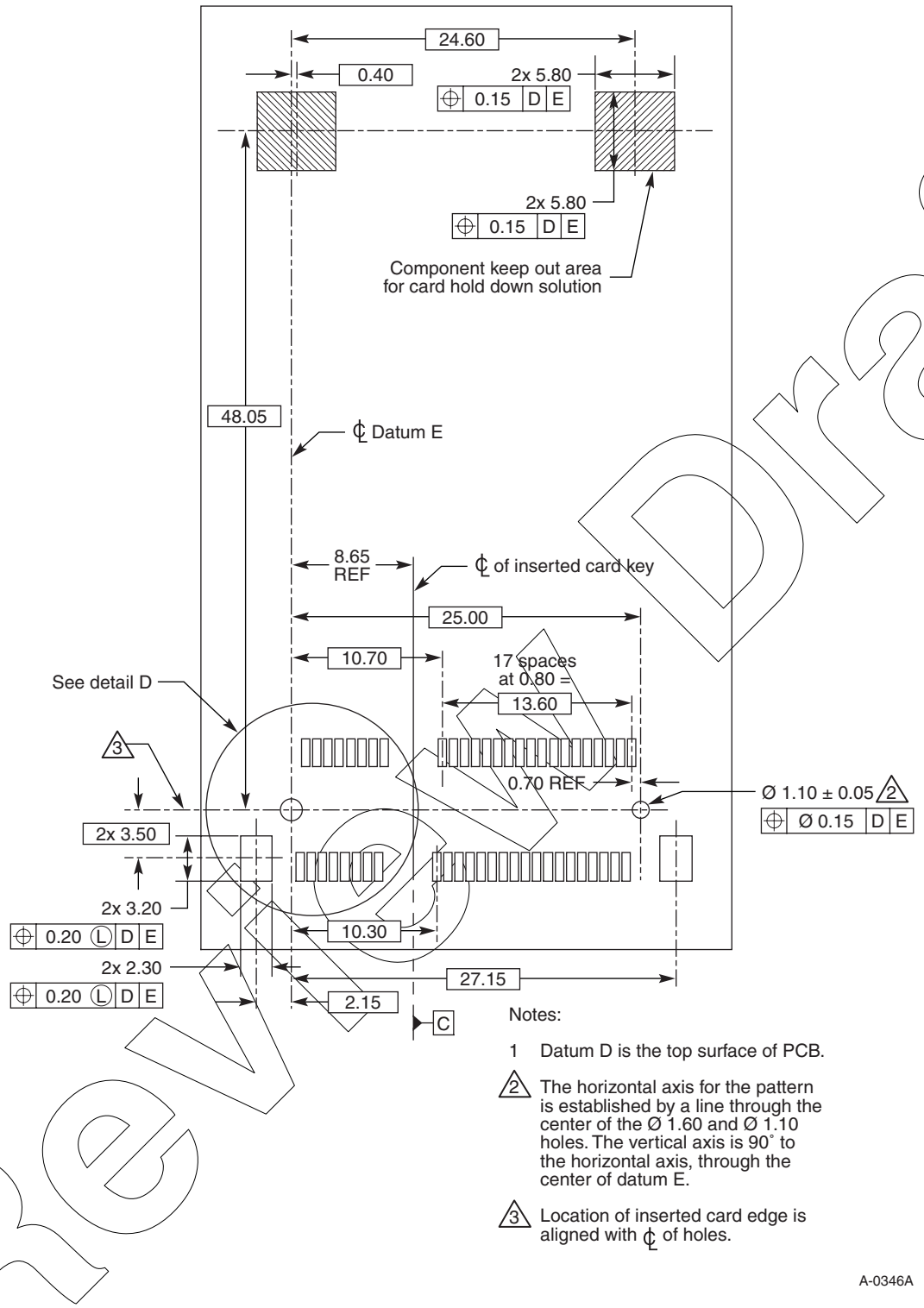

Figure 2-7: Recommended System Board Layout (Single Socket)

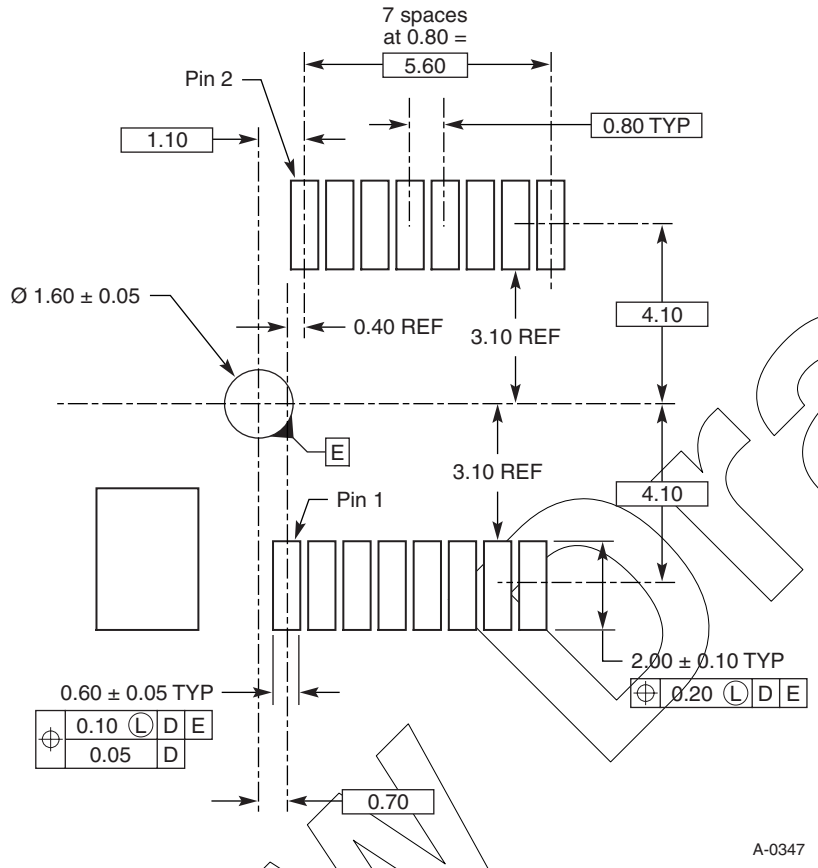

Figure 2-8: Recommended System Board Layout (Detail D)

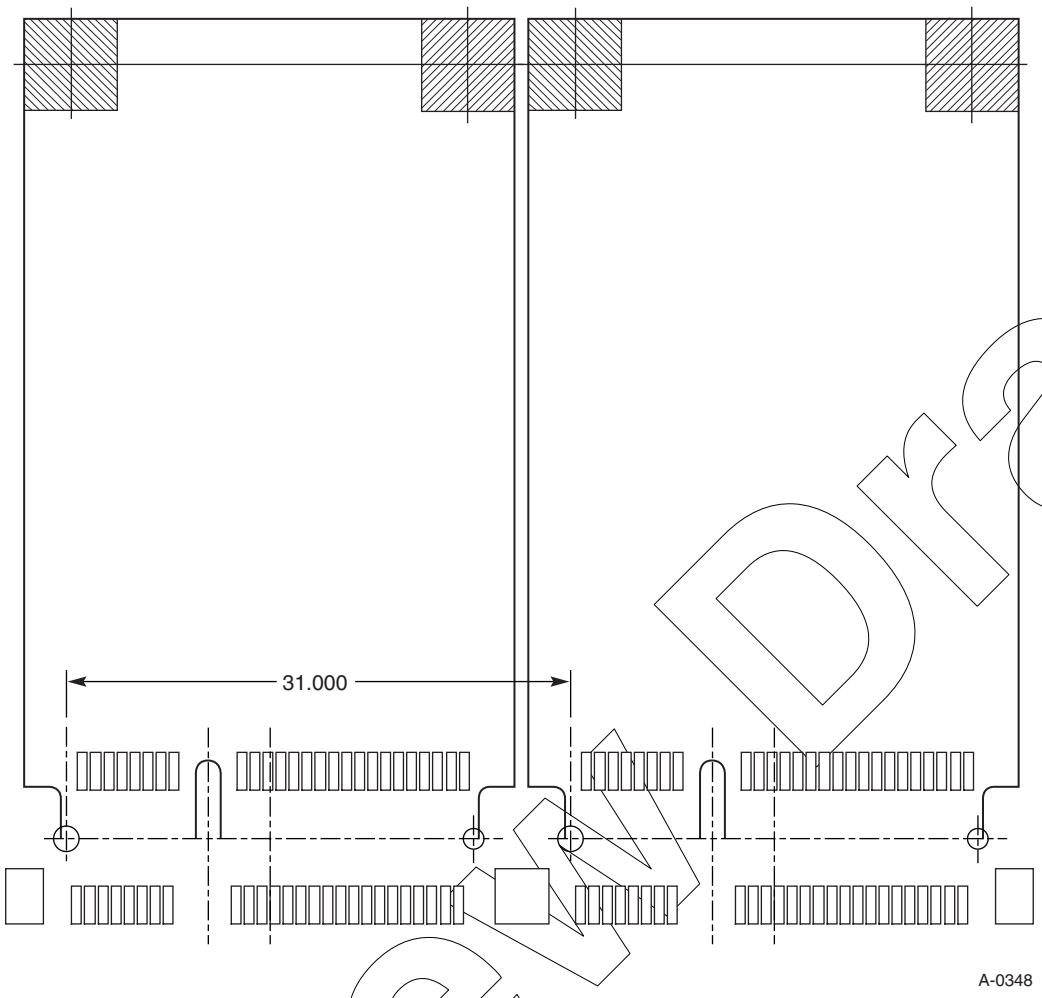

Figure 2-9: Recommended System Board Layout (Dual Socket)

2.3.2. System Connector Parametric Specifications

Table 2-1, Table 2-2, Table 2-3, and Table 2-4 specify the requirements for physical, mechanical, electrical, and environmental performance for the system connector.

Table 2-1: System Connector Physical Requirements

Parameter	Specification
Connector Housing	U.L. rated 94-V-1 (minimum) Must be compatible with lead-free soldering process
Contacts: Receptacle	Copper alloy
Contact Finish: Receptacle	Must be compatible with lead-free soldering process

Table 2-2: System Connector Mechanical Performance Requirements

Parameter	Specification
Durability	EIA-364-9 50 cycles
Total mating/un-mating force*	EIA-364-13 2.3 kgf maximum
Shock	EIA-364-27, Test condition A Add to EIA-364-1000 test group 3 with LLCR before vibration sequence. Note: Shock specifications assume that an effective card retention feature is used.

* Card mating/unmating sequence:
1. Insert the card at the angle specified by the manufacturer.
2. Rotate the card into position.
3. Reverse the installation sequence to unmate.

Table 2-3: System Connector Electrical Performance Requirements

Parameter	Specification
Low Level Contact Resistance	EIA-364-23 55 milliohms maximum (initial) per contact; 20 milliohms maximum change allowed.
Insulation Resistance	EIA-364-21 $> 5 \times 10^8$ @ 500V DC
Dielectric Withstanding Voltage	EIA-364-20 >300 V AC (RMS) @ sea level
Current Rating	0.50 amp/power contact (continuous) The temperature rise above ambient shall not exceed 30 °C. The ambient condition is still air at 25 °C. EIA-364-70 method 2
Voltage Rating	50 V AC per contact

Table 2-4: System Connector Environmental Performance Requirements

Parameter	Specification
Operating Temperature	-40 °C to +80 °C
Environmental Test Methodology	EIA-364-1000.01 Test Group, 1, 2, 3, and 4
Useful field life	5 years

To ensure that the environmental tests measure the stability of the connector, the add-in cards used shall have edge finger tabs with a minimum plating thickness of 30 micro-inches of gold over 50 micro-inches of nickel (for environmental test purposes only). Furthermore, it is highly desirable that testing gives an indication of the stability of the connector when add-in cards at the lower and upper limit of the card thickness requirement are used. In any

case, both the edge tab plating thickness and the card thickness shall be recorded in the environmental test report.

2.3.3. I/O Connector Area

The placement of I/O connectors on a Mini PCI Express add-in card is recommended to be at the end opposite of the system connector as shown in Figure 2-10. The recommended area applies to both sides of the card, though typical placement will be on the top of the card due to the additional height available. Depending on the application, one or more connectors may be required to provide for cabled access between the card and media interfaces such as LAN and modem line interfaces and/or RF antennas. This area is not restricted to I/O connectors only and can be used for circuitry if not needed for connectors.

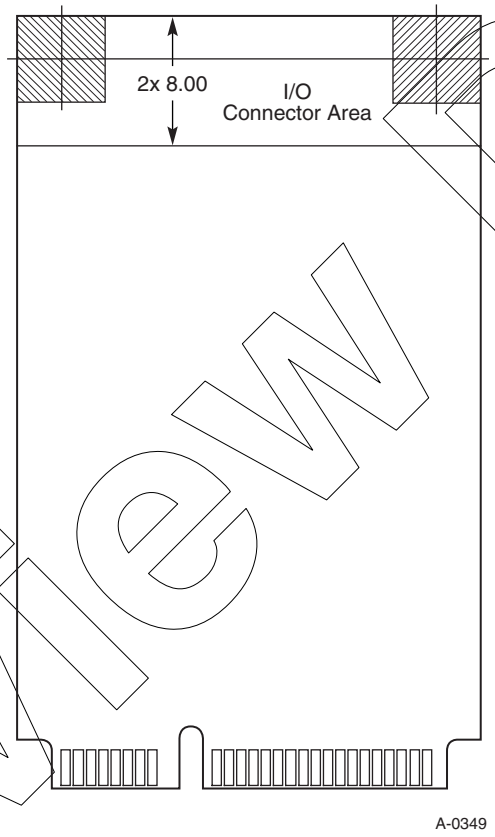

Figure 2-10: I/O Connector Location Areas

2.4. Thermal Guidelines

For purposes of this specification, power consumption is not necessarily directly related to the thermal dissipation limitations within the system; e.g., additional power may be consumed via the system interface, yet the thermal energy may be dissipated in circuits located off the card (most likely in a remote media interface circuit such as an antenna). Power consumption limits for Mini PCI Express are included in Chapter 3.

System Board Requirements:

- System board designers shall ensure that the board can dissipate 28.1 °C/W in the region of the add-in card. The method in which this is dissipated depends on the OEM standards, but natural convection/radiation is unlikely. Most applications will mandate some bleed air of convection over the add-in card.
- Direct attach thermal solutions are not allowed.

Add-In Card Requirements:

- The maximum thermal dissipation directly from any Mini PCI Express add-in card is 2.3 W at a component temperature of 90 °C.
- De-rate maximum card power 0.046 W for every 1 °C component T_{CASE} is rated below 90 °C.
- Example: T_{CASE} = 85 °C, then de-rate power 0.23 W to P = 2.07 W.
- The total thermal energy dissipated must be spread out relatively uniformly over the Mini PCI Express card in order to avoid hot spots. Figure 2-11 provides guidance on power density. The top side of the card can generally tolerate as much as twice the density as the bottom side of the card, with the components on the bottom side being trapped between the add-in card PCB and the system board PCB.

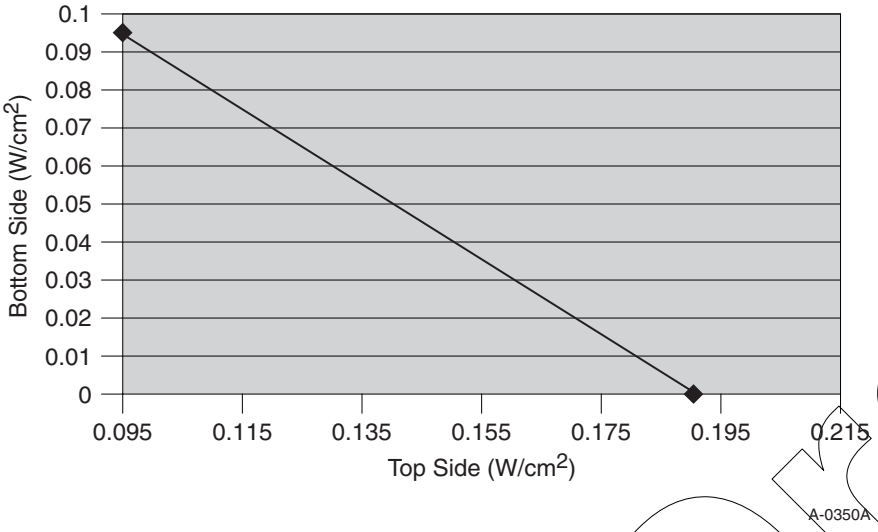

Figure 2-11: Power Density Uniform Loading at 80 Percent Coverage

Example: If side one of the card is loaded to at 0.12 W/cm^2, the other side of the card (side two) can only be loaded to 0.07 W/cm^2. In all cases, the sum of power densities for both sides of the card must not exceed 0.19 W/cm^2.

Note: Additional heat beyond the maximum 2.3 W of thermal dissipation, listed on page 23 as a requirement for an add-in card, may be generated by the Mini PCI Express add-in card's I/O circuitry. For example, for certain modem line conditions in the approved countries, TBR21 states a modem may dissipate as much as 2.4 W additional (40 V drop at 60 mA). If the add-in card requires additional thermal management in order to stay within the aforementioned criteria, the add-in card manufacturer must coordinate with the system board manufacturer to achieve a final solution.

3

3. Electrical Specifications

3.1. Overview

This chapter covers the electrical specifications for Mini PCI Express.

3.2. System Interface Signals

Table 3-1 summarizes the 26 signal and 18 power lines that are supported by the system interface.

Two primary data interfaces are defined for Mini PCI Express: PCI Express and USB. System designers may optionally choose to implement slots that support only one of these interfaces and still be compliant to this specification. As the Mini PCI Express is targeted to BTO/CTO applications, the proper matching of specific add-in cards to systems with the matching data interface has to be managed by the system integrator.

Table 3-1: Mini PCI Express System Interface Signals

Signal Group	Signal	Direction	Description
Power	+3.3V (3 pins)		Primary 3.3 V source
	+1.5V (3 pins)		Primary 1.5 V source
	GND (12 pins)		Return current path
PCI Express	PETp0, PETn0 PERp0, PERn0	Input/Output	PCI Express x1 data interface: one differential transmit pair and one differential receive pair
	REFCLK+, REFCLK–	Input	PCI Express differential reference clock (100 MHz)
Universal Serial Bus (USB)	USB_D+, USB_D–	Input/Output	USB serial data interface compliant to USB 2.0 specification

Signal Group	Signal	Direction	Description
Auxiliary Signals (3.3V Compliant)	PERST#	Input	Functional reset to the card
	WAKE#	Output	Open Drain active Low signal. This signal is used to request that the system return from a sleep/suspended state to service a function initiated wake event.
	SMB_DATA	Input/Output	SMBus data signal compliant to the SMBUS 2.0 specification
	SMB_CLK	Input	SMBus clock signal compliant to the SMBUS 2.0 specification
Communications Specific Signals	LED_WPAN#, LED_WLAN#, LED_WWAN#	Output	Active low signals. These signals are used to allow the Mini PCI Express add-in card to provide status indicators via LED devices that will be provided by the system.

3.2.1. Power Sources and Grounds

Mini PCI Express provides two power sources: one at 3.3V (+3.3V) and one at 1.5V (+1.5V). The auxiliary voltage source (+3.3Vaux) is sourced over the same pins as the primary voltage (+3.3V) and is available during the system's stand-by/suspend state to support wake event processing on the communications card.

3.2.2. PCI Express Interface

The PCI Express interface supports a x1 PCI Express interface (one Lane). A Lane consists of an input and an output high-speed differential pair. Also supported is a PCI Express reference clock. Refer to the *PCI Express Base Specification* for more details on the functional requirements for the PCI Express interface signals.

IMPLEMENTATION NOTE

Lane Polarity

By default, the PETp0 and PETn0 pins (the transmitter differential pair of the connector) shall be connected to the PCI Express transmitter differential pair on the system board and to the PCI Express receiver differential pair on the Mini PCI Express add-in card. Similarly by default, the PERp0 and PERn0 pins (the transmitter differential pair of the connector) shall be connected to the PCI Express receiver differential pair on the system board and to the PCI Express transmitter differential pair on the Mini PCI Express add-in card.

However, the "p" and "n" connections may be reversed to simplify PCB trace routing and minimize vias if needed. All PCI Express receivers incorporate automatic Lane polarity inversion as part of the Link initialization and training and will correct the polarity independently on each Lane. Refer to Section 4.2.4 of the *PCI Express Base Specification* for more information on Link initialization and training.

IMPLEMENTATION NOTE

Link Power Management

Mini PCI Express cards that implement PCI Express-based applications are required by the *PCI Express Base Specification* to implement Link power management states, including support for the L0s and L1 (in addition to the primary L0 and L3 states). For Mini PCI Express implementations, Active State PM for both L0s and L1 states shall also be enabled by default. Refer to Section 5.4 of the *PCI Express Base Specification* for more information regarding Active StatePM.

3.2.3. USB Interface

The USB interface supports USB 2.0 in all three modes (Low Speed, Full Speed, and High Speed). Because there is not a separate USB-controlled voltage bus, USB functions implemented on a Mini PCI Express card are expected to report as self-powered devices. All enumeration, bus protocol, and bus management features for this interface are defined by *Universal Serial Bus Specification, Revision 2.0*.

3.2.4. Auxiliary Signals

The auxiliary signals are provided on the system connector to assist with certain system level functionality or implementation. These signals are not required by the PCI Express architecture, but may be required by specific implementations such as Mini PCI Express. The high-speed signal voltage levels are compatible with advanced silicon processes. The optional low speed signals are defined to use the +3.3V or +3.3Vaux supplies, as they are the lowest common voltage available. Most ASIC processes have high voltage (thick gate oxide) I/O transistors compatible with +3.3V. The use of the +3.3V supply allows PCI Express signaling to be used with existing control bus structures, avoiding a buffered set of signals and bridges between the buses.

The Mini PCI Express add-in card and system connectors support the auxiliary signals described in the following sections.

3.2.4.1. Reference Clock

The REFCLK-/REFCLK+ signals are used to assist the synchronization of the card's PCI Express interface timing circuits. Refer to the *PCI Express Card Electromechanical Specification* for more details on the functional and tolerance requirements for the reference clock signals.

3.2.4.2. PERST# Signal

The PERST# signal is asserted to indicate when the system power sources are within their specified voltage tolerance and are stable. PERST# should be used to initialize the card functions once power sources stabilize. PERST# is de-asserted when power is switched off and also can be used by the system to force a hardware reset on the card. The system may also use PERST# to cause a warm reset of the add-in card. Refer to the *PCI Express Card Electromechanical Specification* for more details on the functional requirements for the PERST# signal.

3.2.4.3. WAKE# Signal

The WAKE# signal is an open drain, active low signal that is driven low by a Mini PCI Express function to reactivate the PCI Express Link hierarchy's main power rails and reference clocks. Only add-in cards that support the wakeup process connect to this pin. If the add-in card has wakeup capabilities, it must support the WAKE# function. Likewise, only systems that support the wakeup function need to connect to this pin, but if they do, they must fully support the WAKE# function. Such systems are not required to support Beacon as a wakeup mechanism. If the wakeup process is used, the +3.3Vaux supply must be present and used for this function. The assertion and de-assertion of WAKE# are asynchronous to any system clock. See Chapter 5 of the *PCI Express Base Specification* for more details on PCI compatible power management. See the *PCI Express Card Electromechanical Specification* for more details on the functional requirements for the WAKE# signal.

Note: The *PCI Express Base Specification* also defines an in-band beacon mechanism to implement wakeup functionality. The WAKE# signal implementation supported here is an out-of-band alternative to the beacon method.

3.2.4.4. SMBus

The SMBus is a two-wire interface through which various system components can communicate with each other and the rest of the system. It is based on the principles of operation of I^2C. The SMBus interface pins are collectively optional for both the add-in card and system board. If the optional management features are implemented, SMBCLK and SMBDAT are both required. The pins assigned to these functions can only be used for these functions and are to be left disconnected if the functions are not implemented. See the *PCI Express Card Electromechanical Specification* for more details on the functional requirements for the SMBus.

3.2.5. Communications Specific Signals

3.2.5.1. Status Indicators

Three LED signals are provided to enable wireless communications add-in cards to provide status indications to users via system provided indicators.

LED_WPAN#, LED_WLAN#, and LED_WWAN# output signals are active low and are intended to drive system-mounted LED indicators. These signals shall be capable of sinking to ground a minimum of 9.0 mA.

Each LED has four defined states as detailed in Table 3-2.

Table 3-2: Defined LED States

State	Definition	Characteristics
OFF	The LED is emitting no light.	
ON	The LED is emitting light in a stable non-flashing state.	
Slow Blink	The LED is flashing at a steady but slow rate.	250 ± 25% milliseconds ON period 0.2 ± 25% Hz blink rate
Intermittent Blink	The LED is flashing intermittently proportional to activity on the interface.	50% duty cycle 3 Hz minimum blink rate 20 Hz maximum blink rate

Table 3-3 defines the recommended use for the LED states for each of the three wireless classes (W-PAN, W-LAN, and W-WAN).

Table 3-3: Recommended Use for LED Indicators by Wireless Classes

State	W-PAN	W-LAN	W-WAN
OFF	Not powered	Not powered	Not powered
ON	Powered; ready to transmit or receive	Powered, associated, and authenticated but not transmitting or receiving	Powered, associated, and authenticated but not transmitting or receiving
Slow Blink	N/A	Powered but not associated or authenticated; searching	Powered but not associated or authenticated; searching
Intermittent Blink	Activity proportional to transmitting/receiving speed	Activity proportional to transmitting/receiving speed	Activity proportional to transmitting/receiving speed For voice applications, turning off and on the intermittent blink based on the ring pulse cycle can indicate a ring event

3.3. Connector Pin-out Definitions

The following sections illustrate signal pin-outs for the system connector. Table 3-4 lists the pin-out for the system connector.

Table 3-4: System Connector Pin-Out

Pin #	Name	Pin #	Name
51	Reserved*	52	+3.3V
49	Reserved*	50	GND
47	Reserved*	48	+1.5V
45	Reserved*	46	LED_WPAN#
43	Reserved*	44	LED_WLAN#
41	Reserved*	42	LED_WWAN#
39	Reserved*	40	GND
37	Reserved*	38	USB_D+
35	GND	36	USB_D-
33	PETp0	34	GND
31	PETn0	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	+1.5V
25	PERp0	26	GND
23	PERn0	24	+3.3V
21	GND	22	PERST#
19	Reserved	20	Reserved***
17	Reserved	18	GND
Mechanical Key			
15	GND	16	Reserved**
13	REFCLK-	14	Reserved**
11	REFCLK+	12	Reserved**
9	GND	10	Reserved**
7	Reserved	8	Reserved**
5	Reserved****	6	1.5V
3	Reserved****	4	GND
1	WAKE#	2	3.3V

* Reserved for future second PCI Express Lane (if needed)
** Reserved for future Subscriber Identity Module (SIM) interface (if needed)
*** Reserved for future wireless disable signal (if needed)
**** Reserved for future wireless coexistence control interface (if needed)

3.3.1. Grounds

Some of the higher frequency signals require additional isolation from surrounding signals using the concept of interleaving ground (GND) pins separating signals within the connector. These pins should be treated as a normal ground pin with connections immediately made to the ground planes within a card design.

3.3.2. Reserved Pins

Reserved pins are not to be terminated on either the add-in card or system board side of the connector. These pins are reserved for definition with future revisions of this specification and are not to be used for non-standard applications.

Three subsets of the reserved pins are tentatively reserved for specific applications as noted in Table 3-4. After all of the generic reserved pins (pins 7, 17, and 19) are defined and, if it is determined that any of these pre-reserved applications are not needed, those specially marked pins may be released for redefinition on an as needed basis.

3.4. Electrical Requirements

3.4.1. Digital Interfaces

A common electrical test fixture is specified and used for evaluating connector signal integrity. The test fixture has 50-ohm single ended traces 6 mils wide that must be uncoupled. The impedance variation of those traces shall be controlled within ±5%. Refer to Appendix A for detailed discussions on the test fixture.

Detailed testing procedures, such as the vector network analyzer settings, operation, and calibration are specified in Appendix A. This appendix should be used in conjunction with the PCI Express Connector Test Fixture.

For the insertion loss and return loss tests, the measurement shall include 1-inch long PCB traces with 0.5 inches on the system board and 0.5 inches on the add-in card. Note that the edge finger pad is not counted as the add-in card PCB trace. It is considered part of the connector interface. The 1-inch PCB trace included in the connector measurement is a part of the trace length allowed on the system board.

Either single ended measurements that are processed to extract the differential characteristics or true differential measurements are allowed. The detailed definition and description of the test fixture and the measurement procedures are provided separately in Appendix A.

An additional consideration to the connector electrical performance is the connector-to-system board and connector-to-add-in-card launches. The connector through hole pad and anti-pad sizes, as well as trace layout on the system board shall follow the recommendations in the *PCI Express Electrical Design Guidelines*. On the add-in card, the ground and power planes underneath the PCI Express high-speed signals (edge fingers) shall be removed.

Otherwise, the edge fingers will have too much capacitance and greatly degrade the connector performance. More detailed discussion on the add-in card electrical design can be found in Appendix A and *PCI Express Electrical Design Guidelines*.

Table 3-5 lists the electrical signal integrity parameters, requirements, and test procedures.

Table 3-5: Signal Integrity Requirements and Test Procedures

Parameter	Procedure	Requirements
Insertion loss (IL)	EIA 364-101 The EIA standard must be used with the following considerations: 1. The step-by-step measurement procedure is outlined in Appendix A. 2. A common test fixture for connector characterization will be used. 3. This is a differential insertion loss requirement. Therefore, either true differential measurement must be made or post processing of the single ended measurements must be done to extract the differential characteristics of the connector. The methodology of doing so will be covered in Appendix A.	1 dB max up to 1.25 GHz; ≤ [1.6 * (F - 1.25)+1] dB for 1.25 GHz < F ≤ 3.75 GHz (for example, ≤5 dB at F = 3.75 GHz)
Return loss (RL)	EIA 364-108 The EIA standard must be used with the following considerations: 1. The step-by-step measurement procedure is outlined in Appendix A. 2. A common test fixture for connector characterization will be used. 3. This is a differential return loss requirement. Therefore, either true differential measurement must be made or post processing of the single ended measurements must be done to extract the differential characteristics of the connector. The methodology of doing so will be covered in Appendix A.	≤ -12 dB up to 1.3 GHz; ≤ -7 dB up to 2 GHz; ≤ -4 dB up to 3.75 GHz
Intra-pair skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max

Parameter	Procedure	Requirements
Crosstalk: NEXT	EIA 364-90 The EIA standard must be used with the following considerations: 1. The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector. This is reflected in the measurement procedure and adjustments to the procedure should be made accordingly. 2. The step-by-step measurement procedure is outlined in Appendix A. 3. A common test fixture for connector characterization will be used. This is a differential crosstalk requirement between a victim differential signal pair and all of its adjacent differential signal pairs. Therefore, either true differential measurement must be made or post processing of the single ended measurements must be done to extract the differential crosstalk of the connector. The methodology of doing so will be covered in Appendix A.	-32 dB up to 1.25 GHz; ≤ -[32 - 2.4 * (F-1.25)] dB for 1.25 GHz < F ≤ 3.75 GHz (for example, ≤ -26 dB at 3.75 GHz)
Jitter	By design; measurement not required	10 ps max

Notes:

1. A network analyzer is preferred. If greater dynamic range is required, a signal generator/spectrum analyzer may be used. Differential measurements require the use of a two-port (or a four-port) network analyzer to measure the connector. The differential parameters may be measured directly if the equipment supports “True” differential excitation. (“True” differential excitation is the simultaneous application of a signal to one line of the pair and a 180-degree phase shifted version of the signal to the second line of the pair.) If single ended measurements are made, then the differential connector parameters must be derived from the single ended measurements as defined in Appendix A.
2. If differential measurements are made directly by application of differential signals, the equipment must use phase-matched fixturing. The fixturing skew and measurement cabling should be verified to be <1 ps on a TDR.
3. The connector shall be targeted for a 100 Ω differential impedance, though it is not explicitly specified.

3.4.2. Power

Mini PCI Express has two defined power rails: +3.3V and +1.5V. Table 3-6 lists the voltage tolerances and power ratings for each Mini PCI Express slot implemented in a system.

Table 3-6: Power Ratings

	Voltage Tolerance	Primary Power		Auxiliary Power*
		Peak (max) mA	Normal (max) mA	Normal (max) mA
+3.3V	±9%	1,000	750	250
+1.5V	±5%	500	375	N/A

* This auxiliary current limit only applies when the primary +3.3V and +1.5V voltage sources are not available; i.e., the card is in a low power D3 state.

Definitions:

Peak – The highest averaged current value over any 10-millisecond period

Normal – The highest averaged current value over any 1-second period

A

Appendix A
Supplemental Guidelines for Mini PCI Express Connector Testing

This section provides supplemental guidelines for testing a Mini PCI Express connector. Because the Mini PCI Express connector has a different form factor and pin configuration than the desktop connector, a set of specific test boards has been designed to be used as the test vehicle for the Mini PCI Express connectors.

A.1. Test Boards Assembly

There are three test boards: one baseboard and two plug-in cards. The baseboard has the footprints for the Mini PCI Express connector. One plug-in card is used in insertion loss and return loss measurement. The other plug-in card is used for crosstalk testing.

A.1.1. Base Board Assembly

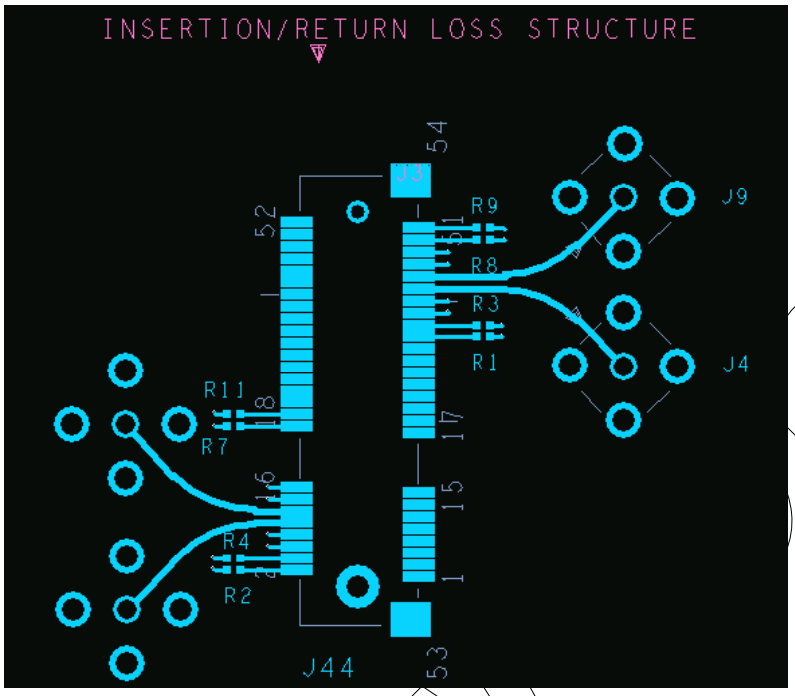

Figure A-1: Base Board Insertion Loss/Return Loss Structure

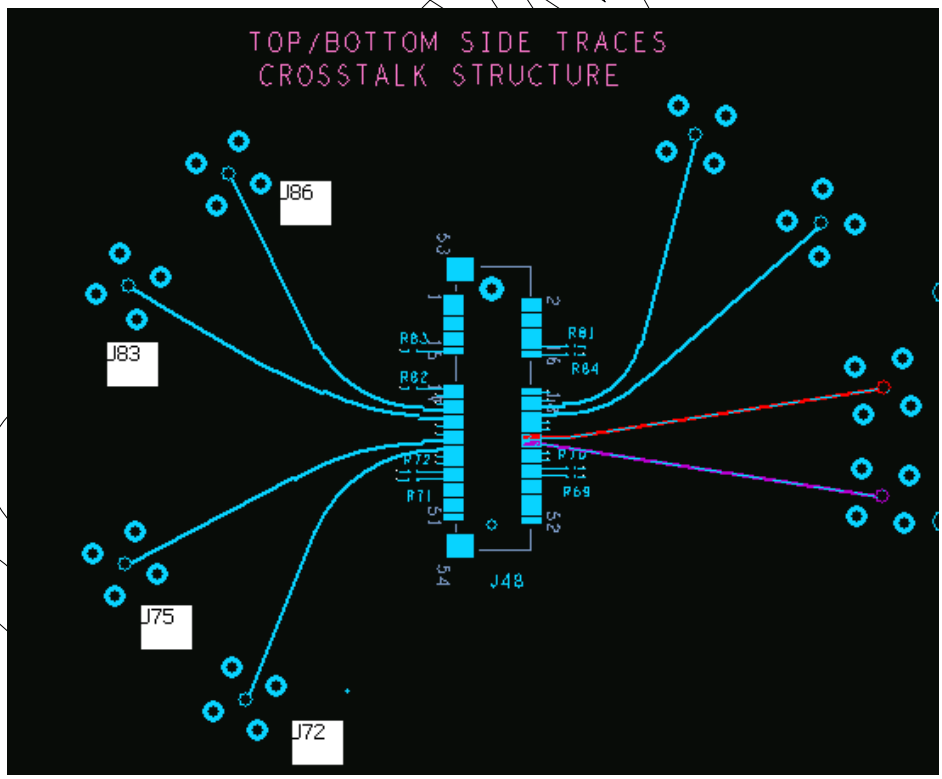

Figure A-2: Base Board Crosstalk Structure

All parts should be on the front side of the baseboard (i.e., the side printed with description of the board). Load the Mini PCI Express connector to location J44 and J48. Load female SMA connectors to locations J4, J9, J72, J75, J83, and J86. Load 0402-SMT 50 Ω resistors to locations R1, R3, R8, R9, R71, R72, R82, and R83.

A.1.2. Plug-in Cards Assembly

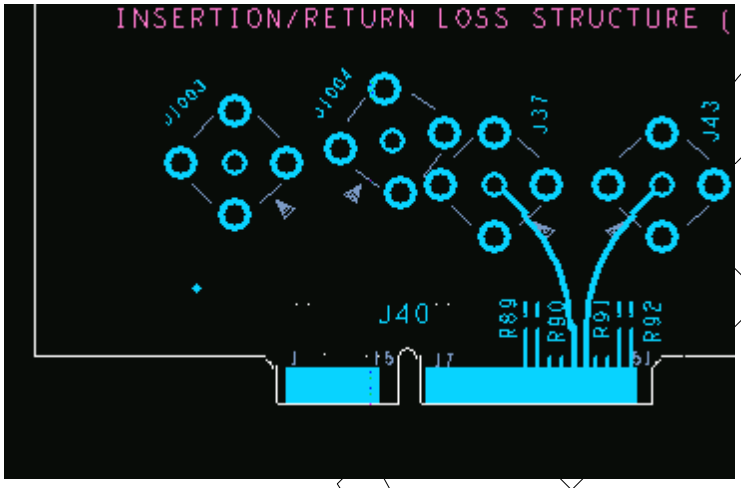

Figure A-3: Plug-in Card Insertion Loss/Return Loss Structure

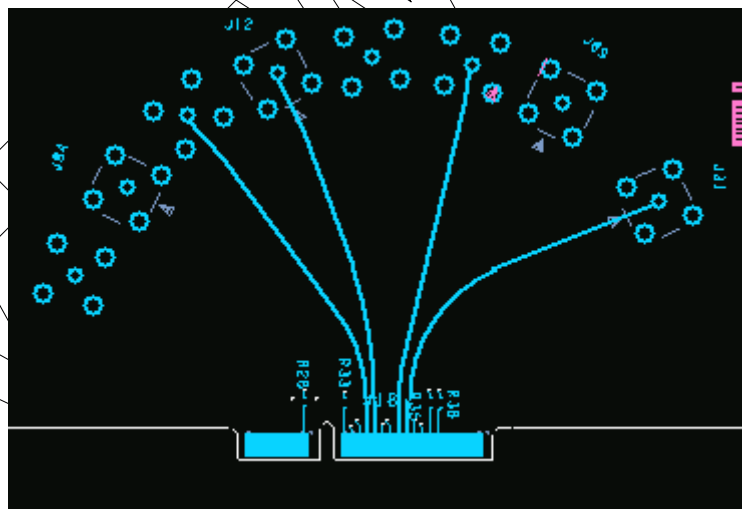

Figure A-4: Plug-in Card Insertion Loss/Return Loss Structure

All parts should be on the front side of the baseboard (i.e., the side printed with description of the board). Load female SMA connectors to locations J37, J43, J12, J31, J8, and J22. Load 0402-SMT 50 Ω resistors to locations R89, R90, R91, R92, R28, R33, R35, and R38.

A.2. Insertion Loss Measurement

Follow the guidelines in Section 5 of the *PCI Express Connector High Speed Electrical Test Procedure*. The mobile test vehicle has the test structures (SMA and traces) as shown in Figure A-1 and Figure A-3.

A.3. Return Loss Measurement

Follow the guidelines in Section 6 of the *PCI Express Connector High Speed Electrical Test Procedure*. The mobile test vehicle has the test structures (SMA and traces) as shown in Figure A-2 and Figure A-4.

A.4. Near End Crosstalk Measurement

Because the Mini PCI Express connector is x1 (one transmit differential pair and one receive differential pair), the near end crosstalk measurement can be limited to the two differential pair. Therefore, the test structure and the mathematics of calculating the near end crosstalk are simplified. The SMA connectors on the board shown in Figure 4 of the *PCI Express Connector High Speed Electrical Test Procedure* can be reduced to the following: J72, J75, J83, and J86. Other neighboring pins on the connector are terminated to 50 Ohm or ground. J72 and J75 form the aggressor pair and J83 and J86 form the victim pair.

Figure A-5 shows the configuration used in mobile measurements followed by an equation to calculate the near end crosstalk. For details on making measurements, refer to Section 7 of the *PCI Express Connector High Speed Electrical Test Procedure*.

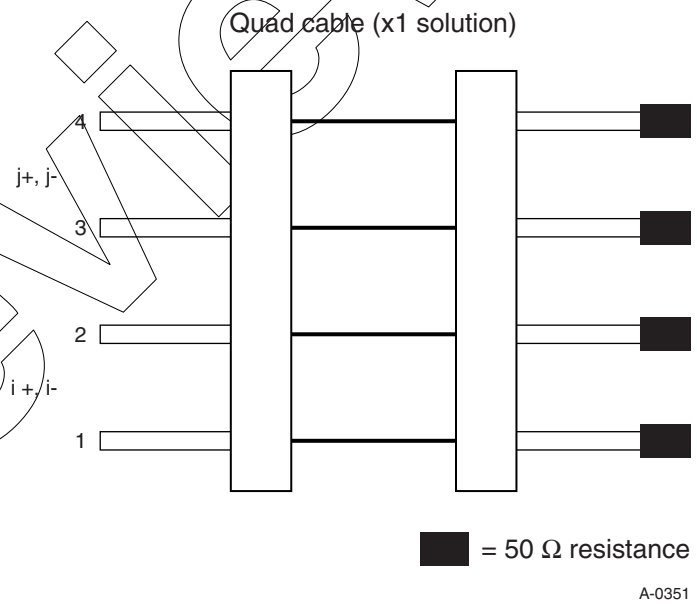

Figure A-5: Near End Crosstalk Measurement Illustration

$$DDNEXT = \frac{1}{2}\left(S_{4\_1} + S_{3\_2}\right) - \frac{1}{2}\left(S_{3\_1} + S_{4\_2}\right)$$

Equation A-1: Simplified NEXT Equation for Mobile

Follow the procedures in Section 8 of the *PCI Express Connector High Speed Electrical Test Procedure* to measure the S-parameters. As a result, substituting the reference designator (J numbers) into Equation A-1, we have

$$DDNEXT = \frac{1}{2}\left(S_{72\_83} + S_{75\_86}\right) - \frac{1}{2}\left(S_{75\_83} + S_{72\_86}\right)$$

Equation A-2: NEXT Equation for Mobile Connector

B

Appendix B
I/O Connector Guidelines

This appendix provides supplemental guidelines regarding available I/O connectors that have been successfully used for applications intended for Mini PCI Express.

B.1. Wire-line Modems

I/O connector recommendations for wire-line modem applications are provided in Section 5.5.2 of the *Mini PCI Specification, Revision 1.0*.

B.2. IEEE 802.3 Wired Ethernet

For I/O connector recommendations for IEEE 802.3 wired Ethernet (LAN) applications, refer to Section 5.5.2 of the *Mini PCI Specification, Revision 1.0*.

B.3. IEEE 802.11 Wireless Ethernet

The following commercially-available connectors have been successfully used in Mini PCI wireless applications. Refer to vendor specifications for more information.

Hirose U.FL Series – SMT Ultra-Miniature Coaxial Connectors (www.hirose.com)